IN THE CLAIMS:

Claim 27 is amended herein. New claims 73-80 are added. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-26 (cancelled).

27. (Currently Amended) A method of establishing electrical contact between a semiconductor substrate and a semiconductor device, comprising:

providing a substrate with an overlying ~~covering said substrate with an~~ insulating layer;

etching a hole through the ~~said~~ insulating layer to the~~said~~ substrate;

introducing ~~partially plugging said hole with~~ doped polycrystalline silicon into the hole;

introducing ~~depositing~~ at least one ~~metal~~ titanium layer within the~~said~~ hole over the~~said~~ doped polycrystalline silicon;

introducing at least one non-titanium layer over the at least one titanium layer and within the hole;

siliciding ~~said at least one metal~~ the titanium layer~~, wherein said step of siliciding said at least one metal layer comprises siliciding a titanium layer~~;

nitridizing the non-titanium layer~~said at least one metal layer, wherein said step of nitridizing said at least one metal layer comprises nitridizing a non-titanium layer~~ by exposing the non-titanium layer to a N_2/NH_3 ambient at a temperature of about 360°C; and

forming the~~said~~ semiconductor device over ~~said at least one metal layer, wherein said step of forming said semiconductor device further comprises forming said semiconductor device over said~~ the non-titanium layer.

Claims 28-72 (Cancelled).

73. (New) The method of claim 27, further comprising exposing the the non-titanium layer to a N_2/NH_3 ambient under a pressure of approximately 4.5 torr.

74. (New) The method of claim 27, wherein exposing the non-titanium layer to a N_2/NH_3 ambient comprises exposing a tungsten layer to a N_2/NH_3 ambient.

75. (New) The method of claim 27, introducing doped polycrystalline silicon into the hole comprises filling the hole with doped polycrystalline silicon and subsequently removing a portion of the doped polycrystalline silicon from the hole.

76. (New) The method of claim 75, wherein removing a portion of the doped polycrystalline silicon comprises etching the doped polycrystalline silicon.

77. (New) The method of claim 27, further comprising siliciding the titanium layer prior to introducing at least one non-titanium layer over the at least one titanium layer and within the hole.

78. (New) The method of claim 27, wherein introducing at least one titanium layer comprises selectively depositing the titanium layer on the polycrystalline silicon through chemical vapor deposition.

79. (New) The method of claim 27, wherein siliciding the titanium layer comprises exposing the semiconductor substrate to $TiCl_4$ with a reactive gas and a carrier gas at a temperature about 400° C in a reaction chamber under a pressure of approximately 0.2 to 2 torr while an rf voltage is applied to the reaction chamber.

80. (New) The method of claim 27, further comprising providing an oxidation barrier between the non-titanium layer and the semiconductor device.